REMARKS

Claims 1-16 are presented for examination, of which claims 1, 10, and 13 are in independent form.

No claims have been amended by way of the present response.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Specification

Paragraph [0002] of the specification of the present application is amended by this response to provide the missing application number and filing date of the related application referenced therein.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

Part A

Claims 1, 3-7, 10, 13, and 14 are rejected in the pending Office Action under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2004/0004975 to Shin et al. (hereinafter the *Shin* reference), in view of U.S. Patent Publication No. 2001/0040908 to Locker et al. (hereinafter the *Locker* reference). In connection with these rejections, the

Examiner commented as follows with respect to the base claims 1, 10, and 13:

> Consider **claims 1, 10, 13** Shin et al. clearly disclose and show a system for effectuating the transfer of data blocks including a header block (fig. 4 (410), fig. 5 (500 header); paragraph 9 (large header)) across a clock boundary (asynchronous clock boundary) between a first clock domain (paragraph 9 (transmitter's clock domain)) and a second clock domain (paragraph 9 (receiving device's local clock frequency)), wherein said first clock domain is operable with a first clock signal (paragraph 9 (transmitter's clock domain)) and said second clock domain is operable with a second clock signal (paragraph 9 (receiving device's local clock frequency)), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M>1 (paragraph 73 (transmitter's frequency is faster than the receiver's (an overrun condition))), comprising: a first circuit portion (fig. 2 (201 transmitter; fig. 3)) for providing said data blocks including said header block to a second circuit portion (fig. 2 (202 receiver; fig. 3)); control logic associated with said second circuit portion for processing said header block (fig.3; paragraphs 3 and 83 (control the transmission and reception of the symbols)).
>
> However, Shin et al. do not specifically disclose the sending of hint signal to accommodate for the longer delay caused by the processing of the header.
>
> In the same field of endeavor, Locker et al. clearly shows the sending of hint signal (paragraph 28 (B sends the hint signal to A for resynchronization because of the clock skew problem. A receives the signal and will make the necessary delay.)).

> Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a system for data transfer, as taught by Shin et al., and demonstrate the use of hint signal, as taught by Locker et al., so that data transfer between two clock domains is done efficiently.

Applicant respectfully traverses the foregoing §103(a) rejections and offers the following discussion as support. As defined by base claim 1, an embodiment of the present disclosure is directed to a system for effectuating the transfer of data blocks across a clock boundary between a first clock domain and a second clock domain, wherein the first clock domain is operable with a first clock signal and the second clock domain is operable with a second clock signal. A first circuit portion provides the data blocks including a header block to a second circuit portion. The claimed embodiment includes, *inter alia*, control logic for processing the header block and for generating, in response to the header block, a hint signal that is operable to be transferred via a synchronizer at least one data cycle prior to the transfer of the data blocks to a third circuit portion disposed in the second clock domain. The claimed system also includes a control block associated with the third circuit portion, the control block operating responsive to the hint

signal to generate data transfer control signals for controlling the third circuit portion in order to control output of the data blocks in a particular ordered grouping. Substantially similar features are also recited in base claims 10 and 13.

The *Shin* reference is directed to a serial communications architecture for communicating between hosts and data store devices. See Abstract. Without acquiescing in the overall characterization provided in the pending Office Action with respect to the *Shin* reference, Applicant simply notes the Examiner's acknowledgment that the *Shin* reference does not disclose the sending of a hint signal as currently claimed. In that regard, Applicant respectfully maintains that the *Locker* reference does not cure the deficiencies of the *Shin* reference, and reliance on *Locker*, therefore, is of no avail for purposes set forth in the pending Office Action.

The *Locker* reference is directed to cross-coupled phase lock loop circuits that provide pseudo-synchronization between two independent clock signals. See Abstract. In the embodiment cited in the §103 rejection, not only are the two clock signals synchronized to each other, but they are also synchronized to a common system clock.

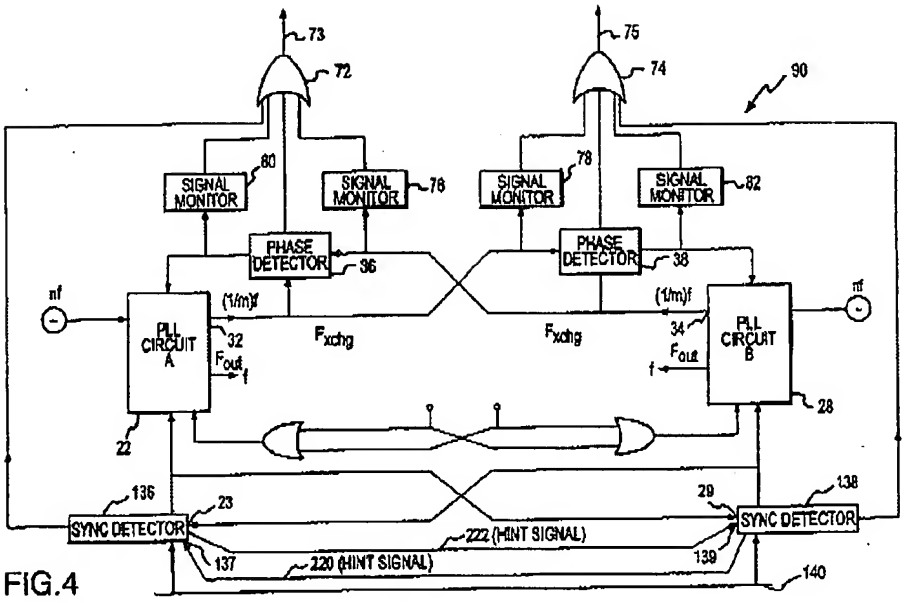

FIG.4

FIG. 4 of *Locker*, reproduced herein for convenience, discloses system 90, which maintains pseudo-synchronization between clock signal F_{out} of PLL circuit A and clock signal F_{out} of PLL circuit B. These two F_{out} clock signals provide redundancy in a communications system and the pseudo-synchronization requires that not only do the two clocks maintain synchronization (within allowable skew) on their edges, but the clocks must also remain in the same clock cycle. Phase detectors 36, 38 monitor the relationship between sampling signals F_{xchng} 32, 34 and, when one of these signals lags behind the other, retards the phase of the

leading clock signal as necessary so that the two output signals are brought back into approximate synchronization. See Paragraphs [0015], [0016], and [0024].

Additionally, the *Locker* reference also maintains synchronization between clocks F_{out} A and F_{out} B and a common system clock by synchronizing to a sync signal carried on synchronization bus 140. Because synchronization bus 140 also carries other signals, the sync signal must first be decoded, so synchronization to a rising edge of the sync signal is not practical. Instead, synchronization is achieved at a predetermined time following the detection and decoding of the sync signal, with each of sync detectors 136, 138 using a respective counter that is triggered by the detection of a sync signal. Because of possible skew between the respective clocks used in channel A and channel B, however, the counts used for system synchronization may not be the same for the two channels when the signal is received close to the boundary between two cycles. In this instance, channel A may detect the sync signal as being in one clock cycle and channel B may detect the sync signal as being in another clock cycle. To maintain the pseudo-synchronization, sync detectors 136, 138 send hint signals 220,

222 to each other to ensure that both clocks will synchronize together. See Paragraphs [0024]-[0027]. To the extent the present Office Action attempts to identify hint signals 220, 222 with the hint signal recited in base claims 1, 10, and 13 of the instant patent application, Applicant respectfully submits that it would be a mis-characterization to make such an identification because, at a minimum, hint signals 220, 222 are not transferred via a synchronizer at least one data cycle prior to the transfer of respective data blocks, as currently claimed. Nor does any circuitry in the *Locker* reference operate in response to the hint signal to generate data transfer control signals in order to control output of the data blocks in a particular ordered grouping, as claimed by Applicant. The *Locker* reference is not concerned with data transfer operations between two different clock domains. Instead this reference is directed to maintaining two clock signals in pseudo-synchronization with each other and in synchronization with a system clock. Accordingly, it is respectfully asserted that the hint signals of the *Locker* reference are not used in a data transfer operation and do not operate to control the ordering of data blocks. Rather, the hint signals of the *Locker* reference are used to maintain pseudo-

synchronization between two clock signals while synchronizing with a third clock signal.

At least for the foregoing reasons, at a minimum, the combination of the *Shin* and *Locker* references fails to teach or suggest all the limitations the pending base claims, a prerequisite for establishing a *prima facie* case of obviousness. Additionally, even if one attempted to incorporate the hint signal of *Locker* into the serial communications architecture of *Shin*, these references do not disclose or suggest a manner in which such a hint signal might be used to control the ordering of data blocks.

Accordingly, Applicant respectfully submits that base claims 1, 10, and 13 are not anticipated or suggested by the applied art of record, and are therefore in condition for allowance. Claims 3-7 depend from base claim 1 and introduce additional limitations therein. Likewise, claim 14 depends from base claim 13 and introduces additional limitations therein. Accordingly, these dependent claims are also believed to be allowable.

Part B

Claims 2, 8, 9, 11, 12, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the *Shin* reference in view of the *Locker* reference and in further view of U.S. Patent Publication No. 2004/0024946 to Naumann et al. (hereinafter the *Naumann* reference).

Applicant respectfully traverses the foregoing §103(a) rejections and offers the following arguments for support. Each claim mentioned in this rejection depends from one of base claims 1, 10, and 13 and contains the distinguishing features of their respective base claim. The present Office Action has conceded that the *Shin* reference is deficient with respect to the features relating to the use of a hint signal. As discussed in Part A above with respect to the §103(a) rejections of the base claims, hint signals 220, 222 of the *Locker* reference are not transferred via a synchronizer at least one data cycle prior to the transfer of respective data blocks, as claimed by Applicant. Nor does any circuitry in the *Locker* reference operate in response to the hint signal to generate data transfer control signals in order to control output of the data blocks in a particular ordered grouping. These combined deficiencies of the *Shin* and *Locker*

references are not cured by the *Naumann* reference, however. *Naumann* is directed to providing communications for system on chip (SOC) configurations, and more particularly to a scalable on chip network (OCN) that enables and manages data operations between multiple processing elements integrated on an integrated circuit (IC) or chip. See Abstract and Paragraph [0001]. As such, *Naumann* does not disclose or suggest the generation of hint signals that are transferred via a synchronizer at least one data cycle prior to the transfer of respective data blocks. Nor does *Naumann* disclose or suggest that in response to the hint signal, control signals are generated in order to control output of the data blocks in an ordered grouping.

Based on the foregoing, Applicant respectfully submits that claims 2, 8, 9, 11, 12, 15, and 16 are in condition for allowance over the applied art of record.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and/or amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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